Claims

[c1] An integrated circuit comprising:
a substrate;
a feature formed on the substrate, the feature; and
a radiation protection layer covering at least a portion of the feature sensitive to radiation, the radiation protection layer reducing penetration of radiation to the portion of the feature sensitive to radiation to reduce radiation damage to the feature.

SUB A1

[c2] The integrated circuit of claim 1 wherein the feature comprises a ferroelectric capacitor having top and bottom electrodes separated by a ferroelectric layer.

[c3] The integrated circuit of claim 2 wherein the radiation protection layer is located on sidewalls of the capacitor to form spacers.

[c4] The integrated circuit of claim 2 further comprises a plurality of features to form a memory array.

[c5] The integrated circuit of claim 4 wherein the radiation protection layer is located on sidewalls of the capacitor to form spacers.

[c6] The integrated circuit of claim 2 further comprises a plurality of features to form a memory array arranged in series architecture.

[c7] The integrated circuit of claim 6 wherein the radiation protection layer is located on sidewalls of the capacitor to form spacers.

[c8] The integrated circuit of claim 1 wherein the radiation protection layer comprises a material which serve as a barrier to radiation.

[c9] The integrated circuit of claim 8 wherein an insulating layer separates the spacers from the feature.

[c10] The integrated circuit of claim 8 wherein an insulating layer separates the spacers from the feature, the insulating layer serves as a barrier to hydrogen.

[c11] The integrated circuit of claim 8 wherein the radiation protection layer

SUB A17

comprises a material which serve as a barrier to UV radiation.

[c12] The integrated circuit of claim 11 wherein an insulating layer separates the spacers from the feature.

[c13] The integrated circuit of claim 11 wherein an insulating layer separates the spacers from the feature, the insulating layer serves as a barrier to hydrogen.

[c14] The integrated circuit of claim 11 wherein the radiation protection layer comprises a noble metal, oxides, or compounds thereof.

[c15] The integrated circuit of claim 14 wherein an insulating layer separates the spacers from the feature.

[c16] The integrated circuit of claim 14 wherein an insulating layer separates the spacers from the feature, the insulating layer serves as a barrier to hydrogen.

[c17] The integrated circuit of claim 8 wherein the radiation protection layer comprises a noble metal, oxides, or compounds thereof.

[c18] The integrated circuit of claim 17 wherein an insulating layer separates the spacers from the feature.

[c19] The integrated circuit of claim 17 wherein an insulating layer separates the spacers from the feature, the insulating layer serves as a barrier to hydrogen.

[c20] A method fabricating an integrated circuit comprising:
providing a substrate with a feature formed on the substrate; and
forming a radiation protection layer to cover at least a portion of the feature sensitive to UV radiation, the UV radiation protection layer reducing penetration of radiation to the portion of the feature sensitive to UV radiation.